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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,501	10/24/2003	David Walter Flynn	550-466	7230

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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
DINH, NGOC V	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/691,501	FLYNN ET AL.	
	Examiner	Art Unit	
	NGOC V. DINH	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL REJECTION

1. This Office Action is responsive to Amendment filed 10/31/08.

2. Applicant's arguments have been fully considered but are not persuasive.

a) In the remarks, With regard to Woods (PN. 7,058,834), applicants argue in substance that: "the memory 270 used for state saving and state restoring is part of the ISPRM 160 and is not disclosed as the memory used during normal processing operation of the integrated circuit 130".

It's the position of the examiner that Woods teaches this limitation as [the memory 270 … external to the chip, col. 7/21-25; the state of the normal circuitry is accessed … is then stored in a memory, col. 3/12-20; during normal operation, multiplexers select the **normal input to the registers**, col. 6/26-31; mechanism controls scan control lines to **scan out the values** of the storage elements (e.g., **registers**)… This state information is then **stored in a memory**, col. 4/44-47].

With regard to the applicant's argument mentioned above, the applicant is reminded that According to MPEP 2144.04 Section V, B &C that Making Integral or Making Separable is not patentable {In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965); In re Dulberg, 289 F.2d 522, 523, 129 USPQ 348, 349 (CCPA 1961)]

The title of Woods invention speaks for itself: save and restore. If the state of the registers, flip-flop and other storage elements are not stored in a NON VOLATILE memory during normal operation, then "when the period of inactivity is ended, Woods col. 2/1-10", the system has no way to restore the state of the device prior to the period of inactivity.

b) In the remarks, With regard to Langford (PN. 5,115,435), applicants argue in substance that "there is no disclosure … in Langford the test data flowing to or from the memory used in normal operation".

It's the position of the examiner that Langford teaches this limitation as [During normal operation … these buses 14, 16, communicate **address and data information** between IC logic function and a large external system, col. 4/30-40]. "communicate **address and data information"** clearly means that a memory device must be located in the system in order to hold address and data.

The purpose of Langford reference is not for the limitation mentioned above, but it is for the missing limitation "multi-bit wide system bus" that Woods does not teach.

Accordingly, the rejections are respectfully maintained and incorporated by reference as set forth in the last office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9, 11-19, 21, 23-24 are rejected under 35 U.S.C 103(a) as being unpatentable over Woods et al PN. 7,058,834, in view of Langford, II et al PN. 5,115,435.

Claims 1-2 and 13-14, Woods teaches apparatus for processing data, comprising:
a circuit used in processing data [fig. 1], said circuit having one or more nodes [storage elements (e.g., register, flip-flops), col. 4/45-47] for storing one or more data values that together define a state of said circuit [scan-based state save…normal the state is then stored in a memory … inactive state power, col. 3/12-25];
a memory for storing data [270, fig. 2; col. 7/3-6; col. 7/20-25]; and
a state saving controller [scan-based state save, col. 4/22-30; state save mode, fig. 2] coupled to said circuit and path [232, 234, fig. 2; col. 7/7-10; a plurality of external scan-

in pads, col. 7/7-15] and operable in response to a state saving trigger [when the state saving mode signal … is asserted, col. 7/42-46; normal mode, col. 6/25-32; power reduction made, col. 8/31-40] and to generate a sequence of memory write requests [a plurality of external scan-in paths 222 are provided to write test data into storage, col. 7/7-10; the data is ready to be written to the memory 270 in a subsequent write operation, col. 10/11-20] on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable [plurality of external scan-in pads 222… to write test, col. 7/7-15; read/write signal… for writing state information to the memory 270; stored state information is restored, col. 7/42-50; see section 2 above].

Woods does not teach a multi-bit wide system bus coupled to said circuit and said memory, for transferring multi-bit data word between said circuit and said memory in response to memory transfer requests issued upon said system bus.

Langford teaches a boundary scanning process comprises a multi-bit wide system bus [parallel system or sub-system bus, col. 2/49-52] coupled to said circuit and said memory, for transferring multi-bit data word between **said circuit** and **said memory** in response to memory transfer requests issued upon said system bus during normal processing operation [Langford, during normal operation … buses 14,16 **communicate address and data information** between IC **logic function 18** and **larger external system** (not shown), col. 4/30-50].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine Langford to Woos in order to speed up data processing [parallel bus processing].

Woods further teaches:

Claims 2 and 14, circuit is a processor core [circuit not only storing data but also processes data/instruction, ISPRM of the circuit (fig. 20) executes read/write request, col. 5/40-50].

Claims 3 and 15, one or more nodes are each coupled to a respective scan chain cell [fig. 2] within said circuit, said state saving controller being operable in response to said state saving trigger to store said data values within respective scan chain cells [col. 6/50-55] and to serially read said data values from said scan chain cells to form said one or more state saving multi-bit data words [Each component 710 has internal scan circuitry and is capable of being scanned... plurality of signals that can include, for example, a serial-in signal, a serial-out signal, a test clock, and a test mode select signal that are known to those of ordinary skill in the art, col. 11/35-41; scan-based state save, col. 4/22-35; col. 4/38-48; col. 9/11-30; fig. 4].

Claims 4 and 16, a plurality of scan chains each containing a plurality of scan chain cells, said plurality of scan chains operating in parallel [plurality of external scan-in pads 222, col. 7/7-15; fig. 2 shows 222 in parallel] to provide respective bits that together form a state saving multi-bit data word as said plurality of scan chains of serially read [serial-in/serial-out signal, col. 11/35-42].

Claims 5 and 17, scan chain cells are also operable to perform test functions upon said circuit [JTAG, col. 11/43-47].

Claims 6 and 18, circuit is a further memory and said data values are bits of data words stored in said further memory [270, fig. 2].

Claims 7 and 19, memory is coupled to a built-in self-test controller operable to perform self-test operations [JTAG see claim 5 above] upon said further memory and said state saving controller uses said built-in self-test controller to read data values from said further memory to form said state saving multi-bit data words [scan-based state save].

Claims 9 and 21, state saving controller is operable in response to a state restoring trigger to generate a sequence of memory read requests [see claim 1] on said system bus that read said one or more multi-bit state saving data words from said memory via said system bus and write said data values represented by said multi-bit state saving data words to said one or more nodes to thereby restore said state of said circuit [scan test, read/write operation, col. 7/1-25; col. 13/claim 13].

Claims 11 and 23, wherein said state saving trigger comprises execution of a state saving program instruction [scan-based save state].

Claims 12 and 24, state saving trigger comprises initiation of a diagnostic test upon said circuit [JTAG, see claim 5].

4. Claims 8, 20 are rejected under 35 U.S.C 103(a) as being unpatentable over Woods, in view of Langford, and further in view of Perner et al PN. 6,728,799.

Claims 8 and 20, Woods-Langford does not teach data burst mode transfer.
Perner teaches scan chain test with burst mode [col. 2/54-57]
However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine Perner to Woods-Langford system to improve speed of data transmission because burst mode data transmission is a well-known method for data transfer wherein burst mode enable to transfer group of memory words as a page of data, this speed up data transfer.

5. Claims 10 and 22 are rejected under 35 U.S.C 103(a) as being unpatentable over Woods, in view of Langford, and further in view of Borden PN 5,790,561.

Claims 10 and 22, Woods-Langford does not teach multi-bit state saving data words is stored in a user specified region of said memory.
Borden teaches a boundary-scan cells test using a user register [30, fig. 2; col. 3, lines 40-45].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine Borden to Woods-Langford's system in order to implement special user functions [col. 3, lines 45-48].

Conclusion

6. Any response to this action should be mailed to:
Under Secretary of Commerce for intellectual Property and Director of the United States Patent and Trademark Office
PO Box 1450
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or faxed to:
(571) 273-8300, (for Official communications intended for entry).
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PMR) system. Status information for published Applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http//pak-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (571) 272-4191. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Hyung Sough, can be reached on (571) 272-6799.

/N. V. D./
Examiner, Art Unit 2189

/Gary J Portka/
Primary Examiner, Art Unit 2188
January 5, 2009